# A 16-Output 10V Compliant Stimulator ASIC with Sub-10nA Mismatch and Simultaneous ETI Sensing for Selective Neural Stimulation

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***Abstract*—This paper presents a 16-output high-voltage (HV) compliant stimulator ASIC for selective neural stimulation. The ASIC supports temporal interference stimulation (TIS) to achieve high-spatial selectivity without requiring nerve-penetrating electrodes. A novel on-the-fly active CB is proposed since existing charge balancing (CB) solutions cannot be directly applied to TIS. Simultaneous electrode-tissue impedance (ETI) sensing is realized by reusing the CB hardware. The stimulator ASIC, fabricated in 130nm Bipolar-CMOS-DMOS (BCD) technology, occupies 0.29mm² per output and achieves 10V compliance while supporting up to 10mA stimulation current and maintaining TIS steering flexibility. The proposed active CB approach compensates for electrode voltage drift during TIS based on a negative feedback loop, achieving a sub-10nA mismatch current over a wide range of ETIs. The ETI sensing reuses the stimulation current and CB hardware for simultaneous measurements during stimulation, achieving a sensing inaccuracy of ±2Ω. Extensive saline experiments confirm the ability of the ASIC to achieve superior spatial selectivity for stimulation while maintaining proper active CB and simultaneous ETI sensing.**

***Index Terms*—Neural stimulator, high-voltage stimulator, charge balancing, electrode-tissue interface, peripheral nerve stimulation, selective neural stimulation, temporal interference stimulation.**

## I. INTRODUCTION

NEUROMODULATION devices have been used in clinical practice for treating various neurological conditions and are expected to benefit from novel technological advances to address the rapid expansion of the patient population [1]. Modulating the activity of the vagus nerve (VN) as one prominent example of peripheral nerve (PN), can offer the possibility of regulating and repairing essential bodily functions, given that the VN is a key component of the parasympathetic nervous system [2-5]. Recognizing its importance, neural stimulation (e.g. VN stimulation) has been approved by the FDA for the treatment of drug-resistant epilepsy and depression [4] and is being explored for its potential benefits in treating chronic inflammation and arrhythmia, conditions that significantly impact patient quality of life [2-3]. However, current PN stimulation (PNS) techniques are not without limitations. Existing solutions using bipolar or tripolar cuff electrodes [6] stimulate the whole nerve with very poor spatial nerve fiber selectivity. Hence therapies based on traditional cuff electrode stimulation often have many undesired side effects due to the stimulation of non-target areas. To improve spatial selectivity, invasive methods based on transverse intra-fascicular micro-electrodes have been proposed [7]. While such methods can indeed achieve much more targeted stimulation, the necessity to insert electrodes into the nerve can pose significant risks, including nerve damage and subsequent complications, making them unsuitable for long-term chronic therapeutic use [8].

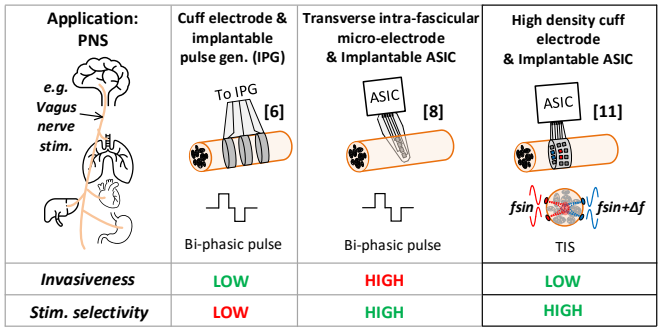


Fig. 1. Comparisons of different approaches for PNS.

To address these challenges, emerging systems leveraging temporal interference stimulation (TIS) have been proposed. Initially applied in the brain [9-10], TIS has later been adapted for PNs [11] to enhance spatial selectivity using non-penetrating electrodes. While TIS is a comparatively new stimulation paradigm and hence its effectiveness is still actively being (pre)-clinically investigated, TIS shows promise in providing side-effect-free PNS [12]. TIS involves the use of 2 differential current stimulators that generate semi-continuous sinusoidal currents in the kHz range with a small frequency offset (e.g. $\Delta f$=10Hz) [9]. Each stimulator requires an independent current source and sink to reduce crosstalk between stimulators. This setup creates an interference pattern within the tissue. Since neural cells are more receptive to low frequency (LF), they would be entrained by the LF envelope [9]. Another attractive feature of TIS is its capability of steering

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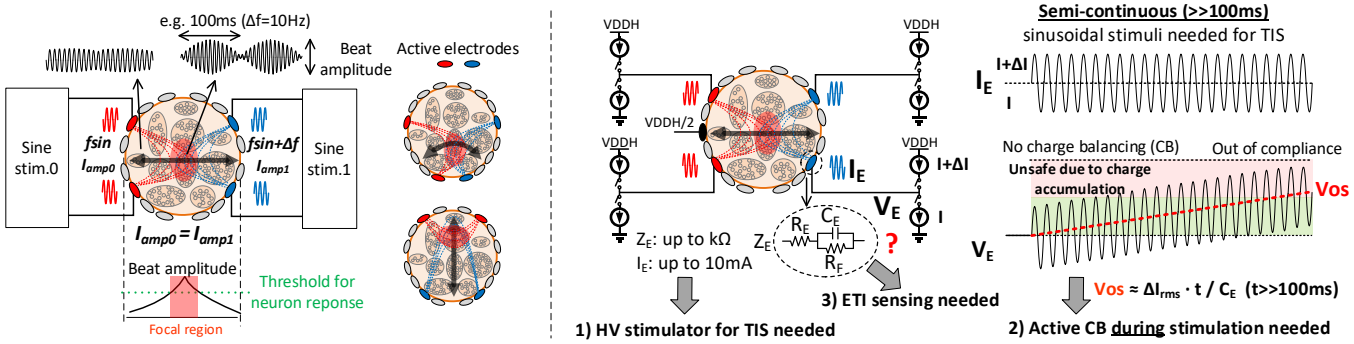



Fig. 2. (left) Illustration of the working principle of TIS (in 2D for simplicity); (right) ASIC requirements for nerve stimulation employing TIS.

the stimulation focal region (i.e. the LF envelope) within the tissue without moving the electrodes. This is achieved by changing the relative stimulation current amplitudes between the 2 stimulation pairs (Fig. 2 left), and the steering direction is determined by the position of the active electrodes. By utilizing a multi-output TIS ASIC with on-chip output selection switches and high-density cuff electrodes, and by carefully selecting the active electrodes at different locations, the stimulation focal region within the PN can be flexibly controlled.

Here we present a neuromodulation ASIC employing TIS that besides spatial selectivity meets the following requirements:

**1) High-voltage (HV) compliance**: For a broad range of therapies, stimulation currents up to 10mA could be needed [5, 13]. However, small cuff electrodes (mm-range diameter) used in PNS have high impedance. For instance, a 1mm diameter platinum black electrode has an impedance exceeding 1kΩ [14], even with the kHz carrier frequency used in TIS. Thus, the stimulator circuit should ideally provide an HV compliance of ≥10V. Together with the multi-output requirement for flexible steering, an area-efficient HV TIS ASIC is essential.

**2) Charge-balancing (CB) during TIS**: CB is crucial for neural stimulators to prevent electrode and/or tissue damage. Unlike the traditional bi-phasic pulse stimulation, TIS is a semi-continuous stimulation method [9]. Taking $\Delta f$=10Hz as an example, a stimulation time >>100ms would be needed to produce a train of LF envelopes. Such long durations mean that even a small mismatch current ($\Delta I$) between the current sink and source would cause significant voltage drift ($V_{os}$) on the electrode (Fig. 2 right). Hence, CB during TIS is necessary for safety, and the mismatch current should be minimized (preferably <<100nA) to prevent $V_{os}$ building up during stimulation [15].

**3) Electrode-tissue impedance (ETI) sensing**: ETI sensing provides vital information about the quality of the electrode as well as the electrode-tissue contact and is often used to assess optimal electrode selection and stimulation parameters. Furthermore, it offers a way to measure implant degradation over time due to for example scar tissue formation [16]. Therefore, ETI sensing with sufficient accuracy is a highly desirable feature.

While TIS ASICs have been demonstrated [10-11], they have low voltage compliance (3.3V), do not support CB during stimulation, nor allow ETI sensing during TIS. To tackle these challenges, we present a 16-output HV TIS ASIC with a novel on-the-fly CB and simultaneous ETI sensing. This paper is an extension of [17]. A prototype is fabricated in 130nm Bipolar-CMOS-DMOS (BCD) technology. The proposed ASIC architecture and stimulator circuit are designed to achieve 10V compliance by leveraging HV transistors in BCD technology. It supports stimulation currents of up to 10mA, while occupies only 0.29mm² per output and maintaining flexibility for TIS steering. The proposed active CB approach monitors the electrode voltages and performs the compensation on the fly with a negative feedback loop at each active stimulator output, achieving a sub-10nA mismatch current. The proposed ETI sensing leverages stimulation current for measurement during stimulation by reusing the CB hardware, achieving ±2Ω accuracy.

The paper is organized as follows. Section II introduces the architecture of the proposed ASIC. Section III details the circuit implementation. Section IV presents the measurement results, and Section V concludes the paper.

## II. ARCHITECTURE

As discussed previously, TIS needs 2 independently controlled differential sinusoidal current stimulators with 4 outputs to realize its basic function. Stimulators with adjustable stimulation current amplitude offer stimulation focal region steering capability. However, this simple system with 4 outputs allows steering of the stimulation focal region in only one direction, since the 4 stimulation electrodes connected to these outputs are fixed in place after implantation. To enable flexible steering of the focal region in multiple directions, the ASIC should support a significantly larger number of outputs (well beyond 4) that can be connected to high-density cuff electrodes and should have the ability to flexibly select the 4 active outputs for TIS. Since the stimulator needs to support HV compliance with a large stimulation current, the transistors in the output stage are large. Therefore, it is important to minimize the number of these components to reduce chip area while keeping the desired output count for flexible TIS steering.

Fig. 3 (top) gives 3 stimulator architecture options for an N× outputs TIS AISC. All the 3 options have 2 independently programmed current DACs (I-DACs), generating the desired sinusoidal currents for TIS. The I-DAC current is then copied

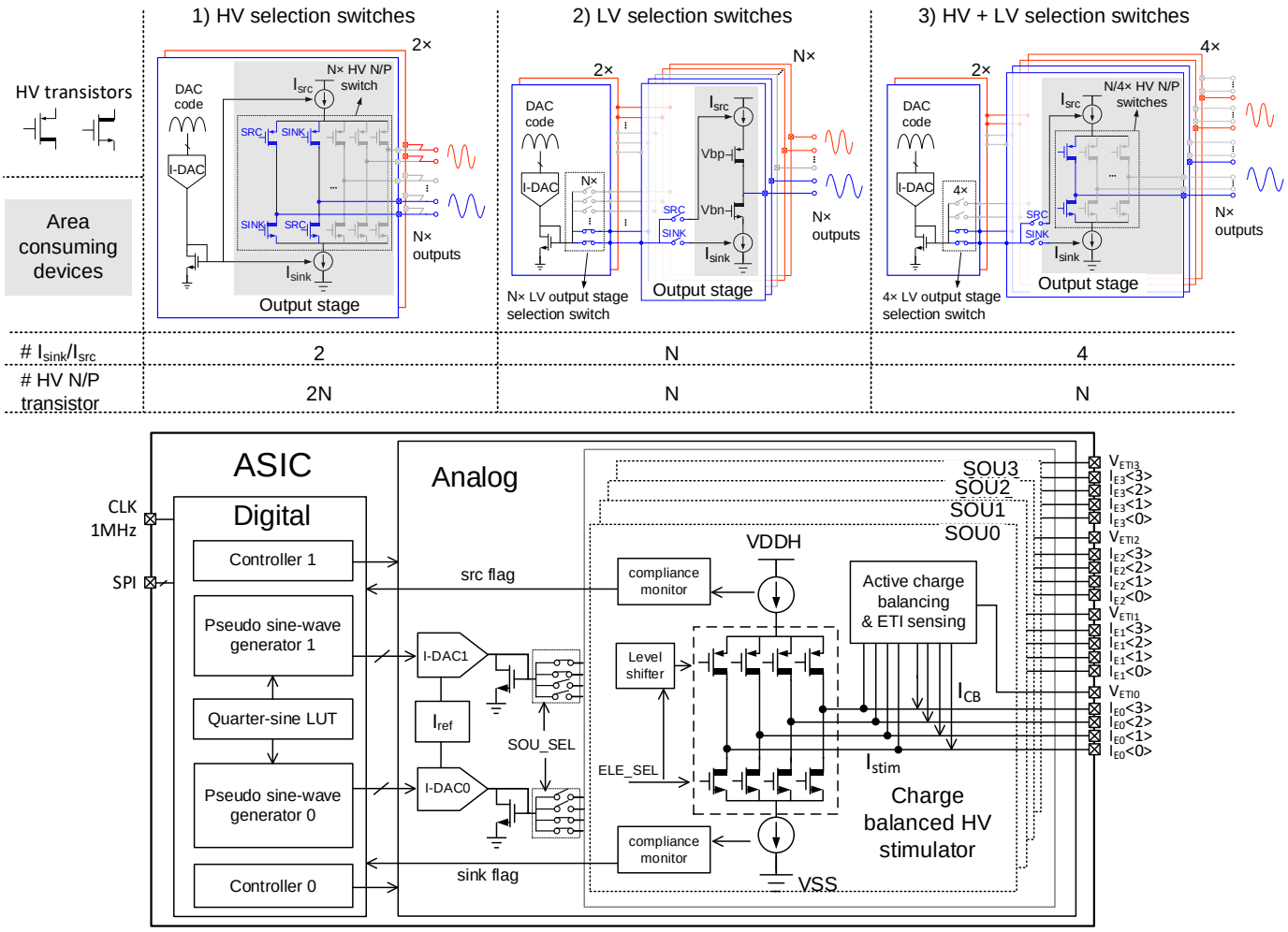



Fig. 3. Comparison of 3 TIS architecture options for N× stimulation outputs; (bottom) the proposed ASIC architecture.

and amplified to the stimulation output stage with current mirrors using low-voltage (LV) devices for better matching with smaller sizes as compared to HV devices. HV devices are then used as cascode transistors to protect the LV devices against HV during operation. The 130nm BCD technology used in this work offers LV (1.5V/3.3V/5V) complementary metal-oxide-semiconductor (CMOS) transistors and HV double-diffused metal-oxide-semiconductor (DMOS) transistors, which can tolerate high drain-source voltages for HV operation. Unless otherwise specified, the terms LV and HV devices refer to the 1.5V CMOS transistors and HV DMOS transistors, respectively. To offer a flexible electrode configuration such that any stimulation output can be selected to produce the sinusoidal current profile from either of the 2 I-DACs, analog switches are needed for active output selection. Note that the outputs that are not selected will remain inactive during stimulation. The first option includes 2× stimulation output stages, and each output stage has N× N- and P-type HV transistors to support N× outputs [18], from which 4 active outputs can be selected. Although this option uses the least number of current sources (2× $I_{sink}/I_{src}$), it requires 2N× HV N/P transistors for flexible output selection, and each HV N/P transistor requires a level shifter for proper switching, which further increases design complexity and chip area. Instead of using complex HV switches, LV switches can be implemented at the gate of the diode-connected transistor that copies the I-DAC current [19], as shown in Fig. 3, the second option. The LV switches then select four output stages, which are configured to operate in two pairs for TIS. As the LV switches only need to drive the gates of the current mirrors, their size is negligible compared to the transistors in the output stage. However, in this case, N× stimulation output stages are needed to support N× outputs. Each output stage contains a pair of $I_{sink}$ and $I_{src}$ and their corresponding HV devices for protection, resulting in a total number of N× $I_{sink}/I_{src}$ and N× HV N/P transistors. The proposed option combines the usage of LV and HV switches to reduce the number of area-consuming devices while offering stimulation output selection flexibility. It includes 4× output stages that work in pairs for TIS, and each output stage contains a 1:N/4 HV demultiplexer (DMUX), supporting total N× outputs. The LV switches select which 2 output stages work in a pair, while the HV DEMUX selects which output within each output stage is active. This approach requires a total of 4× $I_{sink}/I_{src}$ and N× HV N/P transistors. Considering that the size of the HV devices is typically larger than (or at least comparable to) the LV devices used for $I_{sink}/I_{src}$ and that N needs to be much larger than 4 for flexible focal region steering, the proposed architecture is the most area-

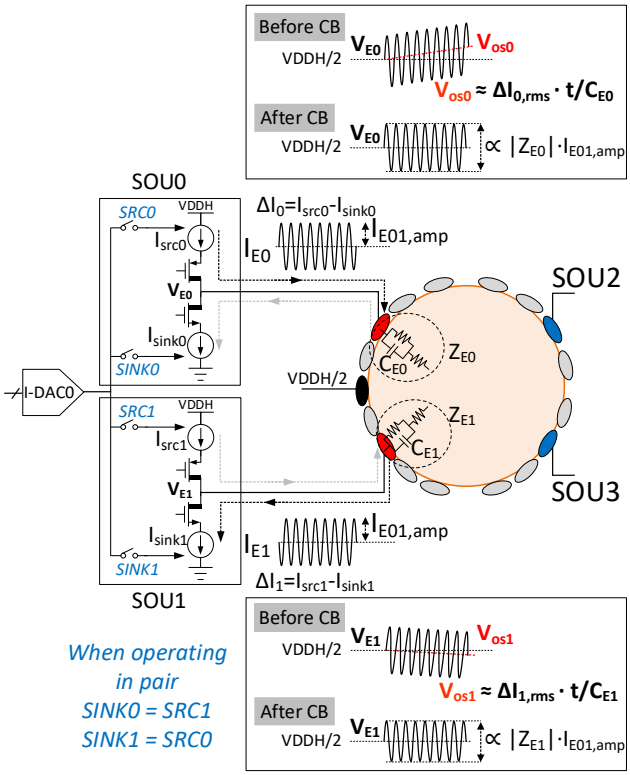



Fig. 4. TIS setup illustration using the proposed ASIC.

efficient choice among these 3 architecture options.

The complete ASIC architecture is shown in Fig. 3 (bottom). It contains 4 stimulation output units (SOU), SOU0-3, and each SOU has an output demultiplexer to 4 electrodes, supporting a total of N=16 electrodes. On-chip digital pseudo-sine synthesizers generate the stimulation current control signals based on a quarter-sine wave look-up table (LUT). Two 9-bit current-steering DACs (I-DAC0/1) similar as in [18], produce the frequency-offset currents which are mirrored into the SOUs. The I-DACs operate on a 1MHz clock to achieve sufficient frequency accuracy and to closely approximate the desired kilo-Hz sinusoidal stimulation current. To offer focal region steering capability, the amplitude of the sinusoidal stimulation current is programmable. This is done by adjusting the I-DAC reference current, which sets the I-DAC's full range from 255.5µA to 1.022mA in 255.5µA increments, thereby adjusting the stimulation current amplitude from 2.55mA to 10.22mA in 2.55mA steps. Optionally, finer adjustments to the stimulation amplitude can be made by modifying the amplitude of the pseudo-sine wave digital signal, though this reduces resolution as the current amplitude decreases. However, these smaller steps provide more precise control for focal region steering. High- and low-side compliance monitoring is implemented in each SOU, which raises a warning flag when the electrode voltage is excessively high or low.

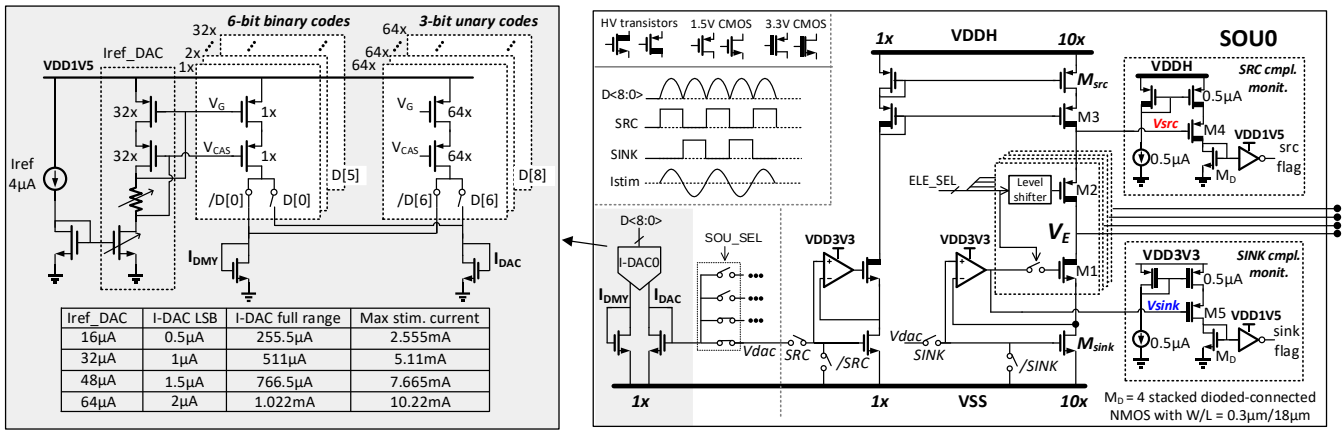
Fig. 4 illustrates how the proposed ASIC is used for TIS. In this example, SOU0/1 and SOU2/3 are used in pairs respectively for TIS, and SOU2/3 and the HV DEMUX in SOU0/1 are omitted for simplicity. When working in a pair, the same stimulation current amplitude and frequency are used for SOU0/1 but with reversed stimulation polarity. This ensures a well-defined current path within the tissue, which is crucial to reduce crosstalk between stimulation pairs for TIS [9]. 2 SOU pairs are synchronized using the same 1MHz clock and the timing of each pair can be independently programmed. A dedicated low-impedance body bias electrode sets the body to *VDDH/2*. Due to the mismatch between $I_{sink}$ and $I_{src}$, each SOU has a random mismatch current ($\Delta I$) being injected into the tissue through the electrode, causing a voltage drift ($V_{os}$) on the electrode depending on the RMS value of $\Delta I$ and the ETI capacitance $C_E$. Therefore, each SOU has its dedicated CB circuit. The use of CB results in stable electrode voltages that can be further used for ETI sensing during stimulation, as described in Section III-C.

## III. Circuit Implementation

### A. I-DAC and HV stimulator

The detailed circuits of the current steering DAC and the HV stimulator and its compliance monitoring circuits are shown in Fig. 5. The I-DAC is implemented with 9-bit resolution and employs a current-steering architecture to reduce spikes caused by code-switching. It is segmented with 3 unary and 6 binary bits to improve linearity, and the least significant bit (LSB) can be programmed from 0.5µA to 2µA by changing its reference current. The current from the LV I-DACs is mirrored (and amplified 10×) to either $M_{sink}$ or $M_{src}$ based on whether the stimulator is operating in sink or source mode. $M_{sink}$ and $M_{src}$ are implemented with LV core devices (1.5V) to save the area. $M_{sink}$ is a standard NMOS device, while $M_{src}$ is an LV PMOS device with extra HV protection rings. The 10× amplification reduces the I-DAC full-scale current to 1.022mA for a maximum stimulation current of 10.22mA. As the I-DAC is operating under a 1.5V supply, its power consumption is thus negligible compared to the HV stimulator. The I-DAC current can be further reduced by increasing the current mirror gain. However, this approach could introduce settling issues with the gate voltage of the current mirror, which would degrade the linearity of the sinusoidal stimulation current.

To provide a sinusoidal current with sufficient linearity (setup with <0.4% THD was used in [9]), the stimulator should have a sufficiently high output impedance, such that the stimulation current is not distorted by the large voltage swing established on the electrode. To boost the output impedance, a regulated HV cascode *M1* is used for $M_{sink}$. *M1* serves two purposes as it at the same time also protects $M_{sink}$ from the HV and forms the HV output DEMUX for electrode selection. To ensure adequate gate voltage to turn on *M1*, the operational amplifier used in the active cascode configuration operates under a 3.3V supply and utilizes thick-oxide LV transistors rated for 3.3V. In principle, the output impedance of $M_{src}$ could similarly be boosted with a regulated cascode structure. However, this would require a floating ground rail (e.g., 3.3V below *VDDH*) to implement the LV operational amplifier used for the regulated cascode device [14]. Instead, $M_{src}$ is protected against HV with a normal cascode HV device M3, and M2 serves as the second cascode device to further boost the output impedance to a sufficient value for linearity and implements the HV DEMUX for electrode selection. It is worth noting that the




| Iref_DAC | I-DAC LSB | I-DAC full range | Max stim. current |
|---|---|---|---|
| 16µA | 0.5µA | 255.5µA | 2.555mA |
| 32µA | 1µA | 511µA | 5.11mA |
| 48µA | 1.5µA | 766.5µA | 7.665mA |
| 64µA | 2µA | 1.022mA | 10.22mA |

Fig. 5. Current steering I-DAC and HV stimulator.

output impedance mismatch between the current sink and source can cause current distortion. However, since both are designed with sufficiently high output impedance, the distortion caused by this mismatch is minimized. Using this topology, the stimulator circuit can operate flexibly from 5V to 12V by simply adjusting the stimulator supply *VDDH*, offering system-level flexibility to save power when possible. An additional HV device M3 is used in each stimulator as compared to the proposed option shown in Fig 3. However, the area overhead is limited, as the number of area-consuming HV devices is increased from 32× to 36× for the 16 outputs of this prototype. The overhead would be even smaller when a larger number of outputs within each SOU is used.

A reference-voltage-free compliance monitor with embedded HV-to-LV level shifting is proposed and implemented for each HV stimulator. When the electrode voltage $V_E$ is abnormally high, $V_{src}$ is pulled towards *VDDH*, turning off *M4* and triggering the high-side compliance flag in the LV domain. The low-side compliance monitor works similarly but checks the output of the regulated cascode amplifier [14] without the need for HV devices. Using this simple structure results in the 2 compliance monitors occupying only 0.02mm$^2$ in total and each consumes only 1µA of current. Unlike the traditional inverter-based configuration [14], the proposed current source compliance monitoring circuit does not require a floating ground, allowing it to operate more flexibly with different VDDH levels and ensuring compatibility with the HV stimulator circuit proposed in this work. While the inverter-based configuration may occupy less area due to its simplicity, the overall area-saving benefit is minimal since the chip area is primarily dominated by the stimulator output stage.

### *B. Charge balancing during TIS*

Due to imperfections in the fabrication process, current mismatches between the $I_{sink}$ and $I_{src}$ must be considered for each SOU [14-15]. Conventional passive CB solutions (Fig. 6(a)), which rely on bulky external capacitors, are impractical for such a system with 16 electrodes due to space limitations. They are also unreliable for alternating current (AC) stimulators, as they can only reject direct current (DC) conduction into tissue [20]. An active CB approach is necessary to effectively compensate for current mismatches.

Several active CB solutions have been proposed for biphasic stimulators [14], [18], [20-25]. Most of them monitor residual voltages at the stimulator outputs after each stimulus and then provide a means of current compensation (Fig. 6(a)). However, since stimulation bursts can be quite long (>100ms) in TIS, charge accumulation can reach unsafe levels during stimulation before it can be detected, as shown in Fig. 2. Detecting $V_{os}$ is particularly challenging due to the continuous nature of sinusoidal waveforms. The unpredictable phase shift between $I_E$ and $V_E$, induced by the ETI at different sinusoidal frequencies, further complicates the timing control for detection. Therefore, existing techniques developed for biphasic current stimulation cannot be directly applied to TIS. In this work, we propose a novel active CB method based on on-the-fly voltage monitoring. During stimulation phases, the voltage drift $V_{os}$ at each active output is monitored and is maintained within safe limits by a feedback loop. Fig. 6(a) shows the implementation of the proposed CB loop. Each CB loop has 4 inputs/outputs, multiplexed to 4 outputs of each SOU. For optimal power and area efficiency, this loop begins with a capacitive divider that generates a scaled copy of the electrode voltage ($V_E$). Before the initiation of stimulation, the output of the capacitive divider is reset to *VREF*, and the stimulator outputs are initially biased to *VDDH/2*, the same as the reference electrode. By choosing an appropriate attenuation factor (*F*), the voltage monitoring circuits can be fully implemented in the LV domain.

As shown in Fig. 2, $V_{os}$ can drift at a rate of $\Delta I_{rms}/C_E$ ($R_F$ is often large) during TIS, with a smaller $C_E$ exacerbating this effect. Since an attenuation factor *F* is applied, the mean voltage of *VSEN* will experience a voltage drift at a rate of $\Delta I_{rms}/(C_E \times F)$ accordingly. The voltage monitoring block needs to extract this near-DC change from the AC voltage signal. A low-pass filter (LPF) could be used for this purpose. However, with the lowest sinusoidal frequency of 1kHz in our application, extracting $V_{os}$ change would require a high-order LPF with a cut-off frequency below 100Hz. The corresponding passive components at these frequencies are impractically large, making LPFs sub-optimal for this application. Instead, as shown in Fig. 6, two peak detectors with complementary architectures [26] are used to

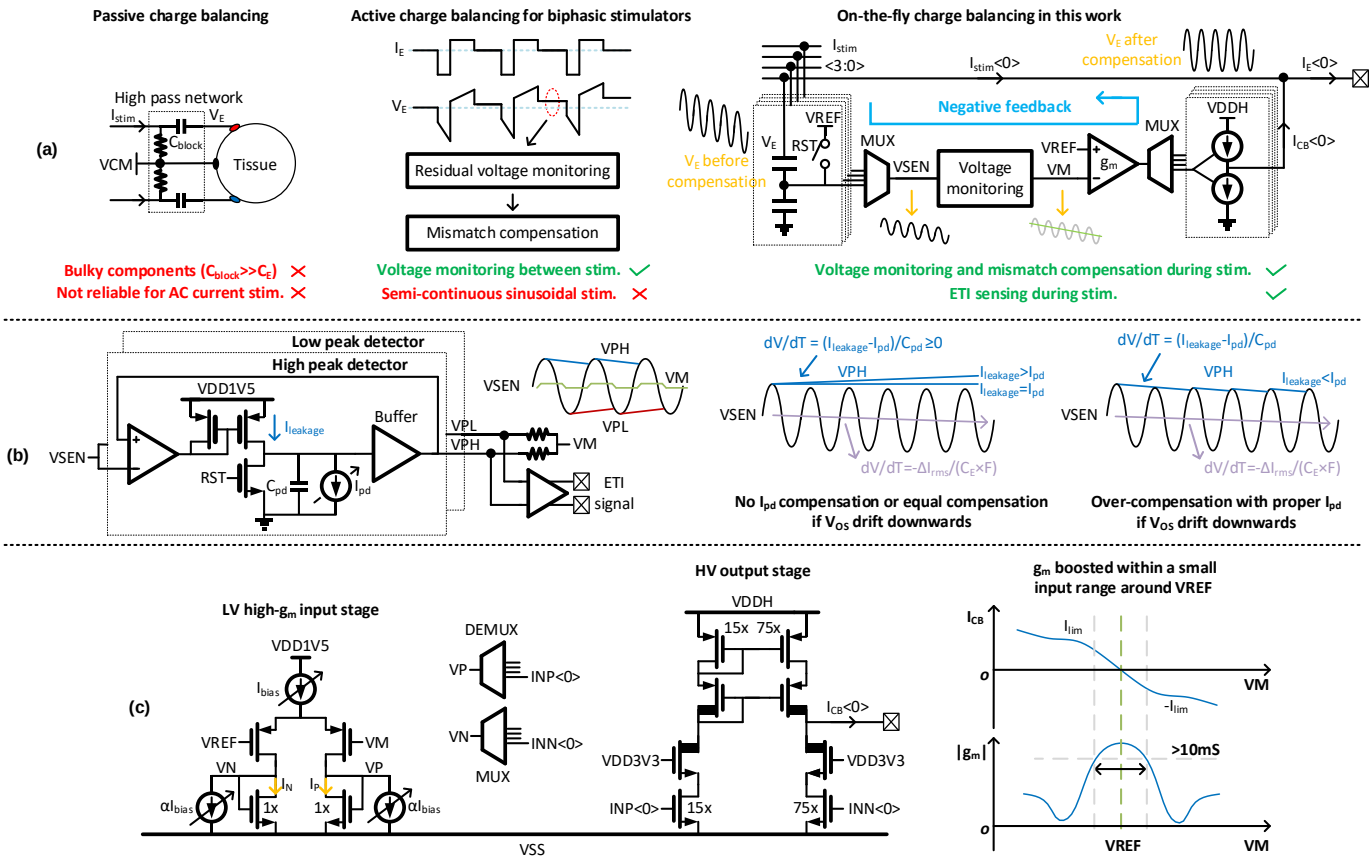



Fig. 6. (a) Comparison of the proposed CB approach with existing solutions in literature; (b) implementation of the voltage monitoring circuit; and (c) implementation of the current-bleeding $g_m$ amplifier.

obtain the peak values (*VPH/VPL*) of *VSEN*. The mean voltage of *VSEN* can be simply generated at *VM* as *(VPH+VPL)/2*. Moreover, the peak information can be further used for ETI sensing as will be explained later.

The operation of the peak detectors can be understood as follows (taking the high peak detector as an example): Initially, $C_{pd}$ (and hence also *VPH*) is reset to ground. As long as *VSEN>VPH*, the pre-amplifier, and current mirror will charge $C_{pd}$ until *VSEN=VPH*, effectively implementing a peak detector. However, leakage from the current mirror ($I_{leakage}$) would continuously increase *VPH*, resulting in an inability to properly track the peak of *VSEN*. To counteract this, $I_{leakage}$ can be over-compensated by using a programmable $I_{pd}$ ($I_{pd}$ >$I_{leakage}$) [27]. In this way, *VPH* always decreases slightly at a rate of $(I_{leakage}-I_{pd})/C_{pd}$, as shown in Fig. 6(b). The use of over-compensation ensures that

$$\frac{|I_{leakage}-I_{pd}|}{C_{pd}} > \frac{|\Delta I_{rms}|}{C_E \times F}, \qquad (1)$$

guaranteeing that *VPH* can accurately track the peak of *VSEN* even if $V_{os}$ drifts downwards.

The stability of this feedback loop relies on timely updating $V_{os}$. As shown in (1), a smaller $C_E$ needs a larger $I_{pd}$ due to the rapid change in $V_{os}$; thus, $I_{pd}$ is programmable to support $C_E$ down to 100nF. However, the use of over-compensation can introduce unwanted ripples at *VPH* and *VPL*, potentially compromising the accuracy of *VM* generation. The ripple amplitude $V_{ripple,amp}$ can be estimated as

$$V_{ripple,amp} \approx \frac{|I_{leakage}-I_{pd}|}{C_{pd}} \times \frac{1}{f_{sin}}, \qquad (2)$$

indicating increased ripple amplitude at a lower frequency. To address this issue, $I_{leakage}$ is minimized to be negligible compared to $I_{pd}$ across PVT variations by using thick transistors, which ensures that the $V_{ripple,amp}$ is mainly influenced by $I_{pd}$ and $C_{pd}$. $I_{pd}$ and $C_{pd}$ are then matched in the two peak detectors, allowing the introduced voltage ripples at *VM* to be suppressed by self-cancellation, as depicted in Fig. 6(b).

*VM* is then compared to a reference voltage (*VREF*) in a transconductance ($g_m$) amplifier. The resulting output current $I_{CB}$ can be expressed as $I_{CB}= g_m \times (VREF-VM)$. Since the change of *VM* reflects $|V_{os}/F|$, larger $g_m$ minimizes $V_{os}$ as in $|I_{CB}/g_m|=|V_{OS}/F|$. It's worth mentioning that during the initial sinusoidal cycles of each stimulation, VPH/VPL will require 1-3 cycles (simulated over PVT variations) to track the peak values and stabilize VM. Therefore, the $g_m$ amplifier is enabled with a programmable delay proportional to the sinusoidal periods. Once the CB loop stabilizes, $I_{CB}$ compensates for the mismatch current $\Delta I$ of the core stimulator, thus $I_{CB}=\Delta I$. In this design, a $g_m$ of more than 10mS over PVT variations is achieved to regulate $V_{os}$ within ~100mV, as per our simulations.

The $g_m$ amplifier consists of two stages: an LV high-$g_m$ input

stage and an HV output stage. The input stage achieves a $g_m$ of ~0.2mS, which is further amplified by a factor of 75× by the output stage. Typically, achieving high $g_m$ requires a large bias current ($I_{bias}$). However, this bias current will be amplified in the output stage through the NMOS current mirror, leading to significant static power consumption from the HV supply. To address this, two current-bleeding sinks ($\alpha I_{bias}$, $\alpha$=10/22) are introduced at the input pair, which can boost the $g_m$ within a small input range around *VREF* while keeping the bias current in $I_P/I_N$ low (~1µA only). As a result, most current consumed by the HV output stage can be used as output current to counteract $\Delta I$. Since $\Delta I$ generally increases with the stimulation current $I_{stim}$, the input stage offers programmable flexibility, enabling power savings for smaller $I_{stim}$.

Fig. 6(c) illustrates the relationship between $I_{CB}/g_m$ and *VM*. Outside of the boosted range, $g_m$ decreases significantly, allowing only a limited output current around $I_{lim}$. $I_{lim}$ is designed to be larger than the 3σ mismatch current of the SOU in the worst case. Therefore, *VM* will be limited around *VREF* when the CB loop is stable and low $V_{os}$ is ensured.

### C. Electrode-tissue impedance sensing

As previously mentioned, ETI sensing offers extra insights into TIS therapies. Typically, ETI sensing involves applying a small current to the electrode and measuring the resulting voltage [28-29]. However, this approach may not be ideal for TIS. To avoid saturation due to stimulation artifacts, sensing is often performed before or after a stimulation pulse train, which could be too sporadic for TIS. Dedicated stimuli and readout circuits are often required, increasing power and area overhead. The additional current injection may also introduce unwanted interactions with the nerve.

In this work, we utilize an added benefit of the proposed CB approach for ETI sensing. Since the peak-to-peak value of the $V_E$ signal inherently correlates with $|Z_E|$ (magnitude of the ETI) multiplied by the stimulation current $I_E$ (Fig. 4), $|Z_E|$ can be derived by leveraging the outputs of the peak detectors as in

$$|Z_E| = \frac{(VPH - VPL) \times F}{2 \times I_{E,amp}}. \quad (3)$$

Since *VPH-VPL* is nearly constant around DC with CB, an on-chip differential buffer (as shown in Fig. 6(b)) can easily output *VPH* and *VPL* as ETI signals without the need for a dedicated readout. Minimal power and area overhead are introduced, making this approach well-suited for TIS.

## IV. Measurement Results

The ASIC is implemented in a 130nm HV BCD technology. A chip photograph with size indications and area breakdown is shown in Fig. 7. The HV stimulator and the active CB & ETI sensing circuit for each SOU occupy 0.51mm² and 0.58mm² respectively for 4 outputs, translating to an area of 0.13mm² and 0.15mm² per output, respectively. The total active area, including all analog blocks, for 16 stimulation outputs is 4.64mm², resulting in an area of 0.29mm² per output. The chip is first characterized with a set of electrical measurements. Saline experiments are then performed by connecting the chip to a nerve cuff electrode. Further, a TIS demonstration is performed in saline showcasing the flexible focal region steering capability of the proposed ASIC.

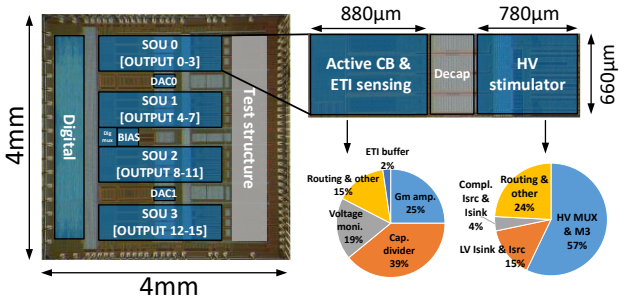



Fig. 7. Die photo with size indications and area breakdown.

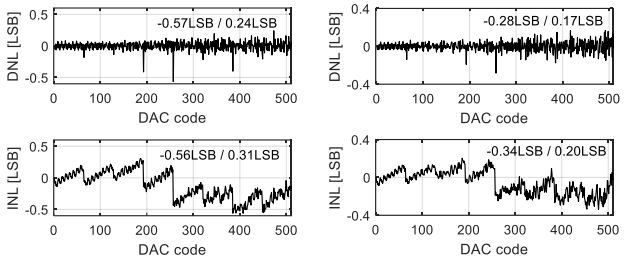



Fig. 8. Measured INL/DNL of I-DAC: (left) $I_{LSB}$ = 0.5µA, and (right) $I_{LSB}$ = 2µA.

### A. Electrical characterization

The static linearity performance of the I-DAC is characterized at its maximum and minimum LSB settings, as shown in Fig. 8. With an LSB current of 0.5µA, the measured integral nonlinearity (INL) and differential nonlinearity (DNL) errors are within -0.57/0.24 LSB and -0.56/0.31 LSB, respectively. These numbers reduce to -0.28/0.17 LSB and -0.34/0.20 LSB when the LSB current is set to 2µA. Fig. 9 (top) shows the DC measurement results of a single SOU by sweeping the stimulator output ($V_E$) from 0 to 12V with a source meter for different current amplitudes. As shown, stable output currents are achieved for both $I_{sink}$ and $I_{src}$ with a worst-case output impedance of >1MΩ. This ensures a <0.5LSB (LSB=20µA) error with a 10V swing on $V_E$, which is crucial for the linearity of the sinusoidal stimulation current and for ETI sensing accuracy. The compliance monitoring reliably triggers when the current drops by ~0.5% from its nominal value. The current source mismatch between $I_{sink}$ and $I_{src}$ is characterized (with CB disabled) at all the 9-bit settings, and the worst-case value is 29µA at 10.22mA (Fig. 9 (bottom left)). Furthermore, the current mismatch is quantified at 10.22mA across 24 SOUs from 6 different chips to obtain the statistical spread, as shown in Fig. 9 (bottom right). Without CB, the measured 3σ mismatch is 103µA at 10.22mA, which is well within the designed $I_{lim}$ in Fig. 6(c) for the active CB.

To evaluate the proposed CB circuit, a sinusoidal stimulation current is generated with a 10.22mA amplitude. To test the CB under worst-case conditions, we deliberately set a 1% mismatch between $I_{sink}$ and $I_{src}$ (hence ~3σ mismatch at 10.22mA). Under these conditions, the electrode voltage $V_E$ is measured from the electrode model. Fig. 10 top demonstrates how the proposed CB regulates $V_{os}$ with $C_E$ = 1µF as an example. With CB disabled,

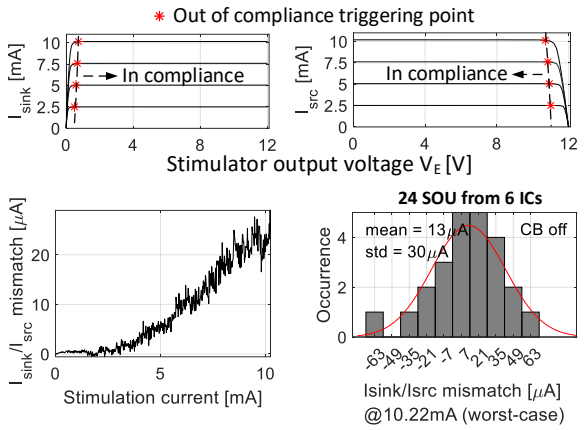
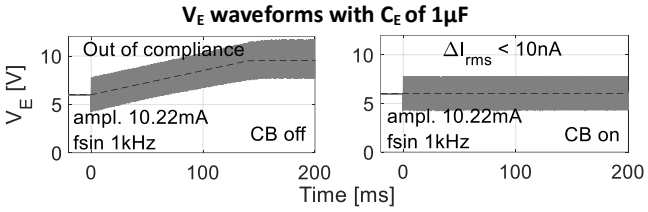



Fig. 9. DC characterization of the HV stimulator.




**Measured CB performance over 1.6s with different $C_E$**

| $C_E$ [nF] | $f_{sin}$ [kHz] | $g_m$ [mS] | $I_{pd}$ [pA] | $I_{stim,amp}$ [mA] | $\|dV_E/dt\|$ [mV/s] | $\Delta I_{rms}$ [nA] | $V_{os,wst}$ [mV] |
|---|---|---|---|---|---|---|---|
| 47 | 1 | 5 | 87.5 | 1.28 | 18 | 0.85 | 10 |
| 47 | 20 | 10 | 12.5 | 10.22 | 7.2 | 0.34 | 28 |
| 1000 | 1 | 10 | 12.5 | 10.22 | 7.2 | 5.7 | 36 |
| 1000 | 20 | 10 | 12.5 | 10.22 | 5.7 | 5.7 | 25 |

Fig. 10. Electrical characterization of the proposed CB with different ETI capacitances.

$V_E$ drifts out of compliance within 200ms at a rate of $|dV_E/dt|$ = 25 V/s, indicating an equivalent RMS mismatch current $\Delta I_{rms}$ of 25μA, calculated as $\Delta I_{rms} = C_E \times dV_E/dt$. When CB is enabled, $|dV_E/dt|$ is reduced to 7.2mV/s, corresponding to an $\Delta I_{rms}$ of 7.2nA. As previously mentioned, the CB loop is optimized for a minimum CE of 100nF in simulations. Here we further evaluate CB performance for $C_E$ values ranging from 47nF to 1μF, with each stimulation lasting up to 1.6s (Fig. 10 bottom). For low frequency and small $C_E$, the amplitude of $I_{stim}$ is reduced to ensure that $V_E$ stays within compliance. $I_{pd}$ is properly chosen based on a lookup table, ensuring that the lowest $I_{pd}$ is provided to maintain good CB performance with minimal voltage ripples at VPH/VPL. Generally, $|dV_E/dt|$ below 20mV/s are achieved, and $V_{os,wst}$ consistently remains below 50mV within 1.6s. For small $C_E$ (47nF) and low frequency (1kHz), $|dV_E/dt|$ is slightly higher. One potential reason is that the voltage ripples introduced by the peak detectors are more significant according to (2), which degrades the feedback loop accuracy. It's important to note that $V_{os}$ may continue to drift with $|dV_E/dt|$ if a longer stimulus is applied. Consequently, the maximum stimulus duration might be constrained by $|dV_E/dt|$ performance to ensure that $V_{os,wst}$ remains within safe limits.

To verify the ETI sensing, different resistors are added to the stimulator output to mimic various tissue impedances. Since *VPH-VPL* is nearly a DC value when the CB loop is stable, its rms value can be measured using a multimeter. Note that as the

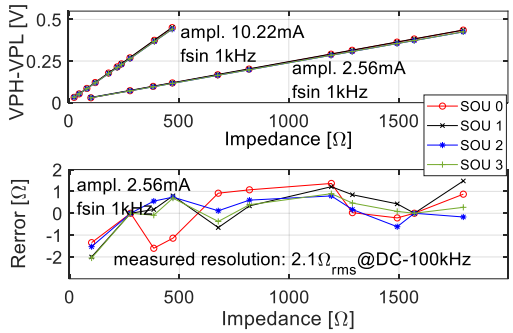



Fig. 11. Electrical characterization of the ETI sensing with stimulation current amplitude of 2.56mA and 10.22mA.

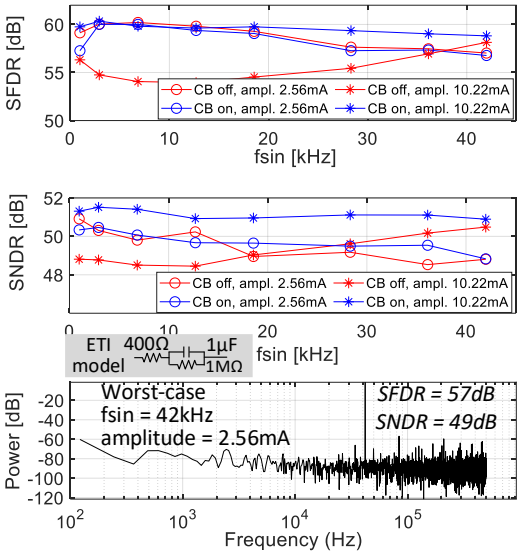



Fig. 12. Measured SFDR (top), SNDR (middle) and spectrum of the stimulation current at worst-case (bottom).

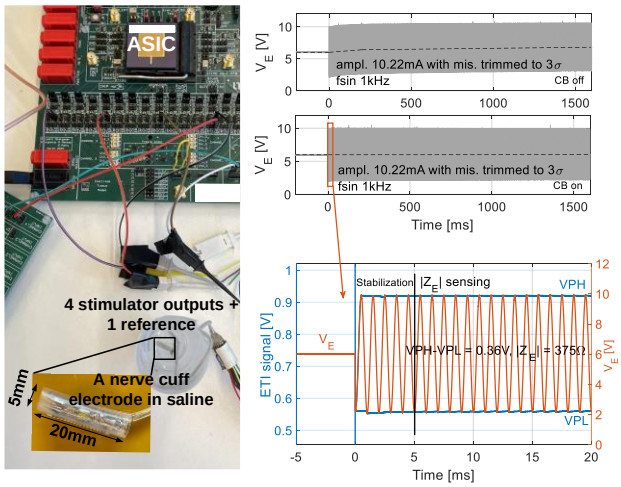



Fig. 13. Characterization of the proposed CB and ETI sensing with a nerve cuff electrode in saline.

proposed ETI sensing method measures only the magnitude of the entire ETI, adjusting the resistor value is equivalent to modifying the ETI magnitude in a more complex R&C model. As mentioned in Section III-B, low frequency leads to larger

ripples at *VPH/VPL*, which can degrade the ETI sensing performance; the characterizations are therefore performed with the lowest sinusoidal frequency of 1kHz. Fig. 11 shows the measured results from 4 SOUs. Smaller current amplitude offers a wider sensing range with reduced accuracy. Impedance values up to 1.8kΩ can be measured using 2.56mA amplitude. After applying a 2-point calibration, an error of ≤2Ω is achieved.

Fig. 12 illustrates the dynamic performance of the generated sinusoidal stimulation current, which is measured using the indicated ETI model. SFDR and SNDR performance with and without enabling CB is compared. The current mismatch is worst at 10.22mA, which can degrade SFDR significantly. Thanks to the CB, SFDR can be further improved with a worst-case of 57dB for frequencies up to 42kHz.

During TIS operation, the chip power is largely dominated by the SOUs which operate at HV domain. For example, with a stimulation current of 10mA per pair, the total chip power is around 175mW, with the SOUs accounting for 96% of this total.

### *B. Saline experiments of CB with a nerve cuff electrode*

A first saline test is performed with a nerve cuff electrode submerged in saline (0.9% NaCl). A sinusoidal stimulation current is generated at 1kHz with 10.22mA amplitude. Fig. 13 shows the CB and ETI sensing performance. The proposed CB approach ensures a small $V_{os}$ (<50mV) over a long stimulation time (1.6s). After the initial settling period, a consistent *VPH-VPL* is established, which is recorded by an oscilloscope as shown in Fig. 13. Since the recorded voltage *VPH-VPL*=0.36V, the measured $|Z_E|$ is 375Ω, which is in line with the expected value for this platinum electrode (size: 1.2mm×1.3mm).

It's worth mentioning here that the CB performance might be compromised due to the inherent characteristics of the ETI (e.g. self-discharging or electrode self-potential), which is a potential limitation for electrode voltage compensation. Therefore, the primary goal of this CB approach is to ensure that the charge on the electrode does not build up and that $V_{os}$ does not increase over time, preventing both electrode and tissue damage.

### *C. TIS demonstration in saline*

Fig. 14 (top) shows a more complicated saline measurement setup specifically designed to validate the stimulation focal steering capability of the proposed ASIC using TIS. A beaker is filled with saline water (0.9% NaCl). 16 stimulation electrodes, which are connected to the chip, and 1 reference electrode (*VDDH*/2) are attached at the circumference of the beaker. The electrode and beaker sizes (1.5cm/10cm diameter) are selected to match the proportions of the small cuff electrodes used around a VN (e.g. ~0.75mm/5mm diameter). TIS is performed with carrier frequencies of 1kHz and 1.01kHz and varying amplitudes. The electric field inside the saline solution is measured in an X/Y fashion [9] with recording probes containing 4 stainless-steel wires spaced 9mm apart. For each grid point (0.5cm pitch) we measured the local differential voltage ($E_x$ and $E_y$) between the recording electrodes X1, X2 and Y1, Y2 for X and Y direction, respectively. The envelope amplitude ($E_{x,\,AM}$ and $E_{y,\,AM}$) of $E_x$ and $E_y$ at the differential

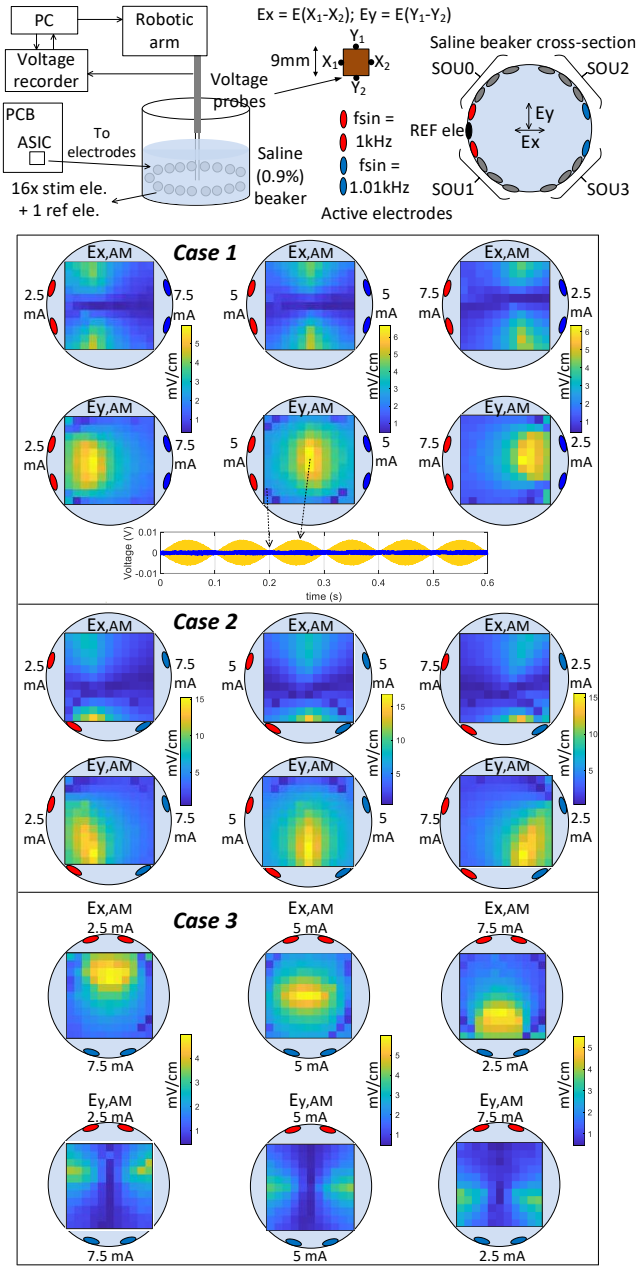



Fig. 14. TIS demonstration of flexible stimulation focal region steering with the proposed ASIC in saline.

frequency of 10Hz is extracted in postprocessing to evaluate the spatial focusing ability of TIS. As shown in Fig. 14, by using different stimulation current amplitudes and electrodes at different locations, the envelope amplitude stimulation focal region can be steered precisely within the area of the 16 electrodes.

It should be noted that, to create detailed TIS focal region steering heatmaps, the size of the phantom and electrodes used in this demonstration is significantly larger than what would be used in real-life applications. Since TIS fundamentally relies on electric fields to shape the desired stimulation focal region [9], the stimulation focal region remains consistent when both the phantom and electrode sizes are scaled together. Therefore, this

Table I. Performance comparison with the state-of-the-art.

| | | This work | [11] ISSCC23[d] | [19] ESSCIRC23[d] | [25] TBCAS24[d] | [22] JSSC18 | [18] JSSC22[d] | [30] CICC21 |
|---|---|---|---|---|---|---|---|---|
| **System** | Technology | **130nm BCD** | 65nm | 55nm HV CMOS | 180nm HV CMOS | 350nm HV | 180nm HV | 180nm HV |
| | Application | **PNS** | PNS | Brain stim | Brain stim | PNS | Brain stim | Brain stim |
| | Selective stim. | **Yes** | Yes | No | No | No | No | Yes |
| | Stim. method/ waveform | **TIS/ Sinusoidal** | TIS/ Sinusoidal | Multipolar/ Bi-phasic | Multipolar/ Bi-phasic | Unipolar/ Bi-phasic | Multipolar/ Bi-phasic | Vector/ Bi-phasic |
| | # Output / # SOU | **16 / 4** | 64 / 64 | 128 / 128 | 4 / 4 | 1 / 1 | 16 / 4 | 46 / 46 |
| | Area [e] / output [mm$^2$] | **0.29** | <0.04 [c] | 0.024 | 3.3 [c] | 2.04 [c] | 1.15 [c] | 0.12 |
| **Stimulator & I-DAC** | Compliance voltage [V] | **10** | <3.3 | <6 | 40 | 22 | 40 | 26 |
| | Compliance monitor | **Yes** | No | No | No | No | No | No |
| | Max amplitude [mA] | **10.22** | 2 | 0.127 | 14 | 5.12 | 12.75 | 2 |
| | I-DAC bit | **9b** | 8b | 7b | 8b | 7b | 8b | 7b |
| | Area / output [mm$^2$] | **0.13** | <0.04 [c] | 0.024 | 2.07 [c] | 1.24 [c] | 0.68 [c] | 0.12 |
| | Max fsin [Hz] | **42k** | >2k | -- | -- | -- | -- | -- |
| | SFDR [dB] | **>57** | -- | -- | -- | -- | -- | -- |
| **Charge balancing** | TIS compatibility | **Yes** | -- | No | No | No | No | No |
| | CB power / SOU [µW] | **60 - 114** [a] | -- | -- | -- | 56 | -- | -- |
| | Area / output [mm$^2$] | **0.15** | -- | -- | 1.06 [c] | 0.8 [c] | 0.3 [c] | -- |
| | CB method | **Active** | -- | Passive | Active | Active | Active | Passive |
| | CB precision | **$I_{mis,rms}$<10nA, $V_{os}$<±50mV** | -- | -- | $V_E$<±2mV/±7.5mV | $V_E$≲±20mV | $V_E$<±2mV | -- |
| **ETI sensing** | Buffer power / SOU [W] | **54µ** | -- | -- | -- | -- | -- | -- |
| | Range [Ω] | **0 – 1.8k** [b] | -- | -- | -- | -- | -- | -- |
| | Inaccuracy [Ω] | **± 2** [b] | -- | -- | -- | -- | -- | -- |

[a] For ±3σ mismatch coverage @ 2.56-10.22mA stim. amplitude, excluding HV compensation current output, which is part of stim. current
[b] @ stimulation amplitude of 2.56mA [c] Estimated from the die photo [d] Only the stimulation circuitry for comparison [e] Including all analog circuitry

scaled setup can still effectively verify the TIS focal region and its steering capability using our ASIC. However, the measured absolute values of the electrical fields in this scaled setup will be much smaller than in actual applications, as the strength of the electric field scales proportionally with $1/d^2$ on a 2D surface, where $d$ is the diameter of the phantom, assuming the stimulation electrodes are scaled and kept at the same relative locations. For example, in case 1 shown in Fig. 14, the measured peak LF electrical field envelope amplitude (EFEA) is slightly above 6mV/cm. Extrapolating this to a high-density cuff electrode placed on a 5 mm diameter peripheral nerve, with the same stimulation parameters, the peak LF EFEA would be approximately 2.4V/cm. However, it is important to note that in real-life scenarios, the LF EFEA also depends on other factors, such as the nerve tissue conductivity (which could differ significantly from the 0.9% NaCl solution used here), stimulation current amplitude, and the relative location of the active electrodes. As a result, stimulation current amplitudes and electrode positions must be carefully adjusted for optimal stimulation efficacy, which remains an important area for further research in TIS [31-32].

### *D. Benchmark*

The performance comparison of the proposed ASIC with prior arts is shown in Table I. This work is the only HV TIS ASIC with a wide programmability of stimulation current and carrier frequency. Thanks to the area-efficient architecture and circuit implementation, an active area of 0.29mm$^2$/output is achieved despite the high stimulation current and HV compliance. An active CB method is proposed for TIS for the first time, achieving a sub-10nA mismatch. ETI sensing during TIS is realized with minimal design complexity.

## V. Conclusion

A 16-output HV ASIC designed for spatially selective neuromodulation through TIS is presented in this work. Fabricated using 130nm BCD technology, the ASIC achieves an area-efficient design. The proposed active CB effectively compensates for mismatch currents during stimulation across a wide range of ETIs. Furthermore, the ETI sensing method demonstrates sufficient accuracy with minimal power and area overhead. Extensive saline experiments validate the ASIC's capability to steer the stimulation focal region based on TIS. Integrating this ASIC in a neuromodulation system would enable novel and more effective electrical neural stimulation therapies, having fewer undesirable side effects, as stimulation can be steered towards the confined neural region of interest.

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